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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,750	11/18/2003	Paul A. Swetland	8486-90994	5530

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,750	SWETLAND, PAUL A.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/27/04pages3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 4 and 21 are objected to for improper antecedent. Claims recites the limitation "said ring". There is not this limitation in claims 1 or 9. There is insufficient antecedent basis for this limitation in this claims.
Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2.1. Claims 1, 5-11, 13–20 and 22-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-17 of U.S. Patent No. 6650548. Although the conflicting claims are not identical, they are not patentably distinct from each other.

All claims of current application teaches "printed circuit board" and claims 1-17 of Patent 6650548 teaches " breadboard " however this limitation in claims 1-17 of patent 66t0548 still reads on all of the claims of current application . A printed circuit board includes particularly a breadboard.

With respect to claims 1, 22 and 14, 20, 23, claims 1 and 12 respectively, of Patent 6650548 teaches all of the limitations exactly except: claim 1 discloses "connection locations" and "conductive strip" and claim 1 of Patent 6650548 teaches " holes" (or "connector clip") and "gang grouping" respectively. "Holes" as usually are "connection locations" of the circuit board.. Claim 1 of Patent 6650548 teaches each grouping being referred to as a conductive trip. As such this limitations in claims 1 and 12 of patent 6650548 still reads on all of the claims 1 and 14 of current application .

Claims 5, 8, 9, 10, 11, 13, 15, 16, 17, 18, 19 correspond to claims 2, 3, 4, 5, 6, 8, 13, 14, 15, 16, 17 of patent 6650548.

With respect to claims 1, 2, 4, 14, 21, claim 1 of patent 6650548 teaches all of the limitations exactly except: claim 1, 12 discloses an insulating plate "having opposite plate surfaces" and claim 18 of 6650548 teaches "plate" but the top and bottom of the insulating plate would be two opposite plate surfaces therefore claim 1 of patent 6650548 reads on claim1, and claim 12 of patent 6650548 reads on claim 14.

Claims 1, 8, 11, 13, 14 also discloses "connections locations", claim 1, 2, 6, 8 of patent 6650548 teaches "holes" which serves the purpose of connection locations therefore claim 1, 2, 6, 8 of patent 6650548 reads on claim 1, 8, 11, 13 respectively.

2.2. Claims 2-4, 6, 7, 12 and 21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 9 of Swetland (Patent No. 6650548 hereinafter "Swetland") in view of Hayward (Patent # 4522449 hereinafter "Hayward").

2.2.1. Regarding claims 2-4 and 21: Swetland discloses the printed circuit board having all of the claimed features as discussed above with respect claim 1(9),

except , Swetland doesn't explicitly teach some of said electrical contact points comprise a metal foil area on at least one of said surfaces with a hole through it's center that extends through said plate and both of said surfaces such that a wire or lead from an electrical component can pass through said hole from the opposite surface of said plate and a soldered connection can be made between said ring and said wire or lead, this technique being commonly referred to as through hole mounting and some of said electrical contact points comprise a solid metal foil area on at least one of said surfaces such that a soldered connection can be made between metal foil said area and a wire or lead from an electrical component that is placed on the same surface as said area, this technique being commonly referred to as surface mounting such that said circuit board can support both said through hole mounting and said surface mounting of wires or leads from electrical components.

Hayward discloses some of said electrical contact points comprise a metal foil area 248, Fig. 8 on at least one of said surfaces with a hole 250 through it's center that extends through said plate and both of said surfaces such that a wire or lead from an electrical component can pass through said hole from the opposite surface of said plate and a soldered connection can be made between said ring and said wire or lead, this technique being commonly referred to as through hole mounting and some of said electrical contact points comprise a solid metal foil area 248, Fig. 8 on at least one of said surfaces such that a soldered connection can be made between metal foil said area and a wire or lead from an electrical component that is placed on the same surface

as said area, this technique being commonly referred to as surface mounting such that said circuit board can support both said through hole mounting and said surface mounting of wires or leads from electrical components. And more, any lands or pads on the circuit board is capable of performing the intended use , then it meets the claims 3 and 4. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963). At time the invention was made, it was well know to use some of said electrical contact points comprise a metal foil area on at least one of said surfaces with a hole through it's center that extends through said plate and both of said surfaces such that a wire or lead from an electrical component can pass through said hole from the opposite surface of said plate and a soldered connection can be made between said ring and said wire or lead, this technique being commonly referred to as through hole mounting and some of said electrical contact points comprise a solid metal foil area on at least one of said surfaces such that a soldered connection can be made between metal foil said area and a wire or lead from an electrical component that is placed on the same surface as said area, this technique being commonly referred to as surface mounting such that said circuit board can support both said through hole mounting and said surface mounting of wires or leads from electrical components.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Swetland discloses to include in his invention that some of said electrical contact points comprise a metal foil area on at least one of said surfaces with a hole through it's center that extends through said plate and both of said surfaces such that a wire or lead from an electrical component can pass through said hole from the opposite surface of said plate and a soldered connection can be made between said ring and said wire or lead, this technique being commonly referred to as through hole mounting and some of said electrical contact points comprise a solid metal foil area on at least one of said surfaces such that a soldered connection can be made between metal foil said area and a wire or lead from an electrical component that is placed on the same surface as said area, this technique being commonly referred to as surface mounting such that said circuit board can support both said through hole mounting and said surface mounting of wires or leads from electrical components to provide easy connection of the different type of the components as taught by Hayward (column 7, lines 7-22).

2.2.2. Regarding claims 6, 7 and 12: Swetland discloses the printed circuit board having all of the claimed features as discussed above with respect claim 5(8),

except, Swetland doesn't explicitly teach the distance of said offset of adjacent rows is a fractional distance no greater than approximately 0.1 inch as claimed claim 6 and distance of said staggering of adjacent rows is a pre-selected distance that is no less than approximately 0.1 inch, as claimed claim 7., and the center-to-center spacing between adjacent rows is approximately 0.05 inch as claimed claim 12.

Although, Swetland doesn't explicitly teach all of this dimensions, Swetland discloses in claim 9 the center-to-center spacing is approximately 0.1 inch. Hayward discloses (column 5, lines 23-30 spacing of the apertures center-to-center is 0.1 inch. A optimum of all of this parameters (dimensions) might be determinate by routine experimentation.

Further, it has been held In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980) . At time the invention was made, it was well know to use the distance of said offset of adjacent rows is a fractional distance no greater than approximately 0.1 inch as claimed claim 6 and distance of said staggering of adjacent rows is a pre-selected distance that is no less than approximately 0.1 inch, as claimed claim 7., and the center-to-center spacing between adjacent rows is approximately 0.05 inch as claimed claim 12.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Swetland to include in his invention that the distance of said offset of adjacent rows is a fractional distance no greater than approximately 0.1 inch as claimed claim 6 and distance of said staggering of adjacent rows is a pre-selected distance that is no less than approximately 0.1 inch, as claimed claim 7, and the center-to-center spacing between adjacent rows is approximately 0.05 inch as claimed claim 12 to provide high density of the breadboard.

Relevant Art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent 2002/0126462 teaches an electrical distribution center provided with a universal cavity design by a multiplicity of terminal-receiving slots. The slots are arranged in laterally spaced parallel rows with the slots in each row in equally spaced apart relation to one another

4.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

4.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

4.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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